REMARKS

This application has been reviewed in light of the Final Office Action dated September 10, 2008. Claims 1–22 are pending in the application. Claim 19 has been amended to correct an informality. Independent claim 22 has been added, and it incorporates subject matter which the Examiner has indicated to be allowable. No new matter is believed to be added. No new issues are believed to have been raised that would require a new search.

By the Office Action, claims 1–19 and 21 stand rejected under U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,506,903 to Yamashita (hereinafter "Yamashita") in view of U.S. Patent No. 6,317,642 to Boyce (hereinafter "Boyce"). Claim 19 is objected to on the grounds of an informality, and Claim 20 is objected to for depending upon a rejected base claim, but is deemed to be allowable if rewritten in independent form.

Claim 1 recites, inter alia, "the transport processor generating a second error signal after receiving the first error signal." Claims 11 and 18 recite analogous language. The Examiner acknowledges that Yamashita does not disclose this element, but asserts that Boyce discloses this element in de-interleaver (507) of Figure 5. Boyce's de-interleaver takes the data words produced by the Reed-Solomon decoder and splits them up into individual bytes. (See Boyce, col. 12, lns 41–46). However, it is respectfully asserted that this cannot properly be considered the generation of a second signal. The de-interleaver simply divides a single, k-byte block of data into k separate bytes — it in no way alters the contents of the signal. By way of contrast, the present specification discloses a means for generating a second error signal which differs from the first error signal. The Forward Error Correction module generates a signal which communicates the fact that a particular packet has an error, while the

transport processor sends out a software packet error signal which begins before and ends after the corresponding data packet. It is evident that the signal emits an error signal that is substantially different (in that particular embodiment, having at least a different duration) from the first error signal. The same cannot be said for the action of Boyce's de-interleaver, which merely passes along the error signal it receives, substantially unchanged. It is therefore respectfully asserted that Yamashita and/or Boyce, taken alone or in combination, fail to disclose or suggest the generation of a second error signal.

It is therefore respectfully asserted that claims 1, 11, and 18 are in condition for allowance. Because claims 2–10, 12–17, 19–21 depend from claims 1, 11, and 18 respectively, it is therefore respectfully asserted that these claims are also in condition for allowance. Based on the Examiner's indication of allowability for claim 20, it is also believed that claim 22 is in condition for allowance.

It should also be noted that certain dependent claims also include allowable subject matter apart from claims 1, 11, and 18. For example, Claim 6 recites, inter alia, "the duration of each logical high frame of the second error signal has a duration greater than the data packet associated with the logical high frame." Claims 14 and 19 include analogous language. The Examiner concedes that Yamashita does not disclose this element, but asserts instead that Boyce discloses this element in column 13, lines 1–7. However, it is respectfully asserted that Boyce never discusses the length of the error signal, and certainly does not disclose or suggest having an error signal of greater duration than the associated data. Boyce explicitly states that every byte where an error is detected is replaced by a "zero" byte or an error code, which means it is exactly the same size as the original data. (See Boyce, col 11, lns 65–67). Even if

the de-packetizer discussed above did generate a second error signal, one skilled in the art will recognize that it cannot produce a signal longer than that fed to it. As a result, it is respectfully asserted that Yamashita and/or Boyce, taken alone or in combination, fail to disclose or suggest a second error signal with a duration greater than the associated data packet.

Claim 22 is new. Based upon the Examiner's indication of allowability for claim 20, it is believed that claim 22 is also in condition for allowance. Claim 20 recites, "A method according to claim 18, further comprising the steps of: starting each discrete second error signal frame before an associated data packet begins; and stopping each discrete second error signal frame after an associated data packet ends." Applicants note that claims 7 and 8 depend from claim 1 and separately include the same subject matter as claim 20, which the Examiner has indicated as allowable. Although Applicants believe that the claims as presented are in condition for allowance, Claim 22 has been introduced to include the language of claims 1, 5, 7 and 8 in the interest of furthering prosecution.

In view of the foregoing arguments and amendments, Applicant respectfully requests that the rejections of the claims be withdrawn, that pending claims 1–22 be allowed, and that the case proceed to early issuance of Letters Patent in due course.

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It is believed that no additional fees or charges are currently due. However, in the event that any additional fees or charges are required at this time in connection with the application, they may be charged to Applicant's representatives Deposit Account No. 07-0832.

Respectfully submitted,
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